WHAT IS CLAIMED IS:

1. A method for block code error correction, the block code including a plurality of data entities in rows and columns and corresponding to an erasing address table and an error table, the erasing address table including a plurality of erasing entities in rows and columns, the error table including a plurality of error entities in rows and columns, the method comprising the steps:

(A) inputting a block code and initializing an erasing address table corresponding to the block code;

(B) decoding the block code in row direction based on the erasing address table in order to find data errors on rows and accordingly update an error table corresponding to the block code;

(C) updating the erasing address table in row direction according to a first determination principle;

(D) decoding the block code in column direction based on the erasing address table in order to find data errors on columns and accordingly update the error table; and

(E) updating the erasing address table in column direction according to a second determination principle.

2. The method as claimed in claim 1, wherein steps (B) to (E) are repeated until no error presents or repeat number is over a predetermined value.

3. The method as claimed in claim 2, wherein in step (C), the first determination principle is applied as the following condition: when

$g_i(e,f)$ is greater than T_R, setting erasing entities of i-th row of the erasing address table as true, where T_R is a first preferred performance parameter, $g_i(e,f) = 2e(i,:) + f(i,:) = 2\sum_{j=1}^{n} \chi(e(i,j)) + \sum_{j=1}^{n} f(i,j)$, n is column number of the block code, $e(i,j)$ is value obtained by decoding error entity of i-th row and j-th column of the error table, $f(i,j)$ is value recorded in erasing entity of i-th row and j-th column of the erasing address table, and $\chi(x) = \begin{cases} 0 & x = 0 \\ 1 & x \neq 0 \end{cases}$.

4. The method as claimed in claim 3, wherein the first preferred performance parameter T_R has values 6, 9, 10, 10, 10 respectively corresponding to iterative numbers 1, 2, 3, 4, 5 for each repeat from step (B) to step (E).

5. The method as claimed in claim 2, wherein in step (E), the second determination principle is applied as the following condition: when $h_j(e,f)$ is greater than T_C, setting erasing entities of j-th column of the erasing address table as true, where T_C is a second preferred performance parameter, $h_j(e,f) = 2e(:,j) + f(:,j) = 2\sum_{i=1}^{k} \chi(e(i,j)) + \sum_{i=1}^{k} f(i,j)$, k is row number of the block code, $e(i,j)$ is value obtained by decoding error entity of i-th row and j-th column of the error table, $f(i,j)$ is value recorded in erasing entity of i-th row and j-th column of the erasing address table, and $\chi(x) = \begin{cases} 0 & x = 0 \\ 1 & x \neq 0 \end{cases}$.

6. The method as claimed in claim 5, wherein the second preferred performance parameter has values 12, 15, 16, 16, 16 respectively corresponding to iterative numbers 1, 2, 3, 4, 5 for each repeat from step (B) to step (E).

7. A device for block code error correction, the block code including a plurality of data entities in rows and columns, the device comprising:

a block code input unit, to input a block code;

an erasing address table having a plurality of erasing entities in rows and columns, wherein the plurality of erasing entities correspond to the plurality of data entities of the block code, respectively;

an error table having a plurality of error entities in rows and columns, wherein the plurality of error entities correspond to the plurality of data entities of the block code, respectively; and

a decoder, to decode the block code in a row direction based on the erasing address table for finding data errors on rows and accordingly updating the error table and further updating the erasing address table in the row direction according to a first determination principle, and subsequently decode the block code in a column direction based on the erasing address table for finding data errors on columns and accordingly updating the error table and further updating the erasing address table in the column direction according to a second determination principle.

8. The device as claimed in claim 7, wherein the decoder decodes the block code for a plurality of times until no error presents or the decoding number is over a predetermined value.

9. The device as claimed in claim 8, wherein the first determination principle is applied as the following condition: when $g_i(e,f)$ is greater than T_R, setting erasing entities of i-th row of the erasing address table as true, where T_R is a first preferred performance parameter, $g_i(e,f)=2e(i,:)+f(i,:)=2\sum_{j=1}^{n}\chi(e(i,j))+\sum_{j=1}^{n}f(i,j)$, n is column number of the block code, $e(i,j)$ is value obtained by decoding error entity of i-th row and j-th column of the error table, $f(i,j)$ is value recorded in erasing entity of i-th row and j-th column of the erasing address table, and $\chi(x)=\begin{cases}0 & x=0\\ 1 & x\neq 0\end{cases}$.

10. The device as claimed in claim 9, wherein the first preferred performance parameter has values 6, 9, 10, 10, 10 respectively corresponding to iterative numbers 1, 2, 3, 4, 5 for each repeat from step (B) to step (E).

11. The device as claimed in claim 9, wherein the second determination principle is applied as the following condition: when $h_j(e,f)$ is greater than T_C, setting erasing entities of j-th column of the erasing address table as true, where T_C is a second preferred performance parameter, $h_j(e,f)=2e(:,j)+f(:,j)=2\sum_{i=1}^{k}\chi(e(i,j))+\sum_{i=1}^{k}f(i,j)$, k is row number of the block code, $e(i,j)$ is value obtained by decoding error entity of i-th row and j-th column of the error table, $f(i,j)$ is value recorded in erasing entity of i-th row and j-th column of the erasing address

table, and $\chi(x) = \begin{cases} 0 & x = 0 \\ 1 & x \neq 0 \end{cases}$.

12. The device as claimed in claim 11, wherein the second preferred performance parameter has values 12, 15, 16, 16, 16 respectively corresponding to iterative numbers 1, 2, 3, 4, 5, for each repeat from step (B) to step (E).